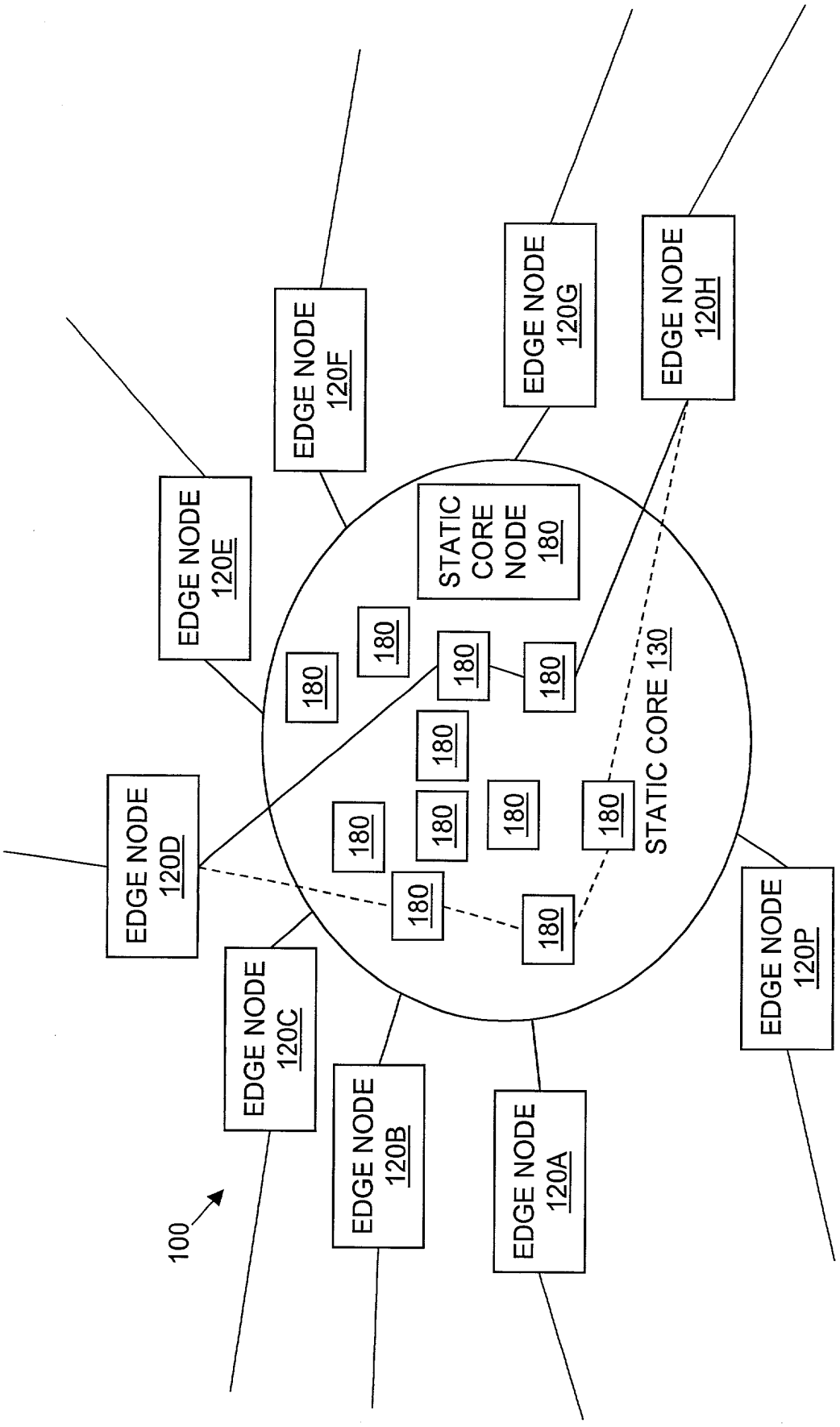
100
EDGE NODE 120A
EDGE NODE 120B
EDGE NODE 120C
EDGE NODE 120D
EDGE NODE 120E
EDGE NODE 120F
EDGE NODE 120G
EDGE NODE 120H
EDGE NODE 120P
STATIC CORE NODE 180
180
STATIC CORE 130

FIG. 1

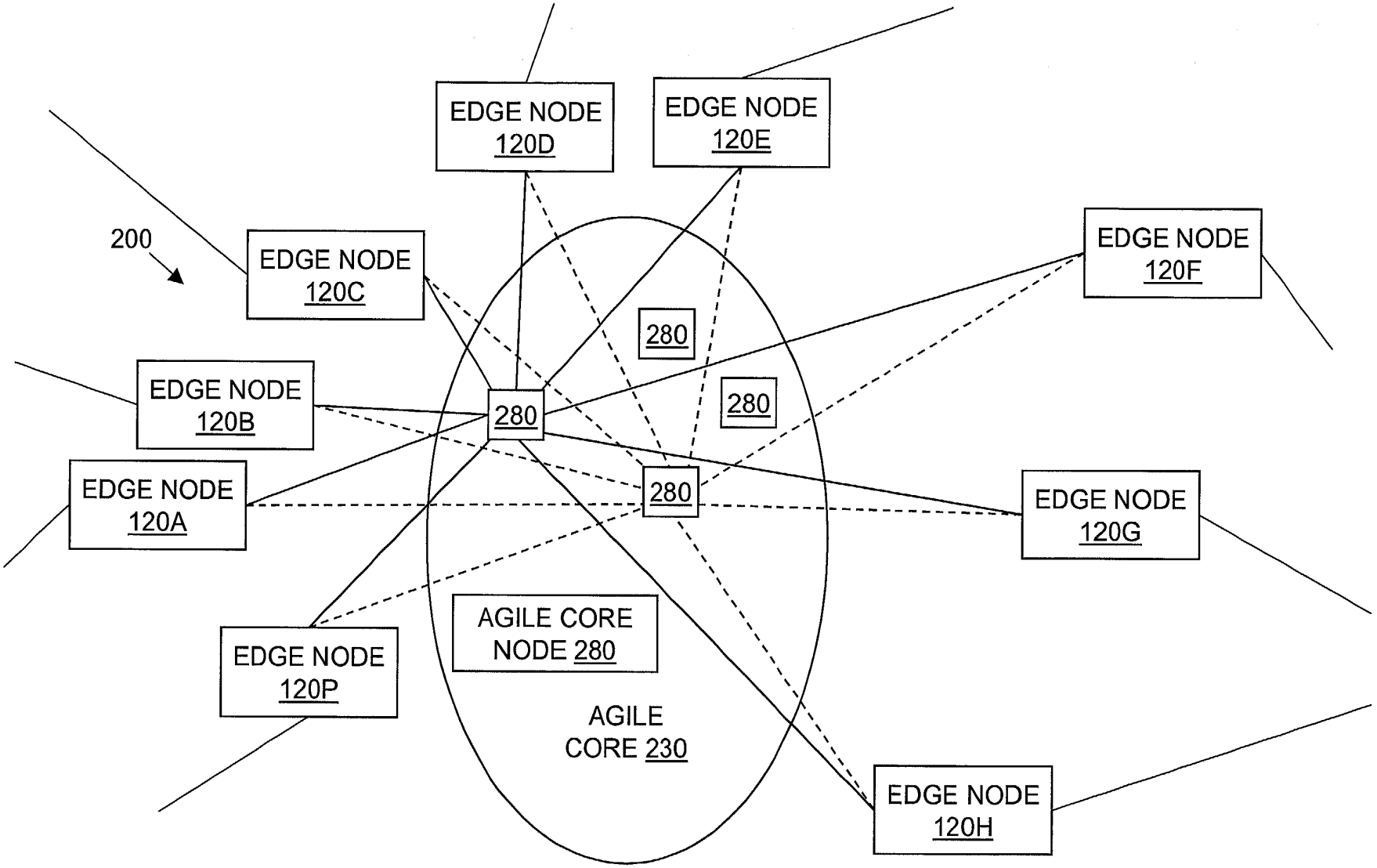
200
EDGE NODE 120D
EDGE NODE 120E
EDGE NODE 120C
EDGE NODE 120F
280
EDGE NODE 120B
280
280
EDGE NODE 120A
EDGE NODE 120G
AGILE CORE NODE 280
EDGE NODE 120P
AGILE CORE 230
EDGE NODE 120H

FIG. 2

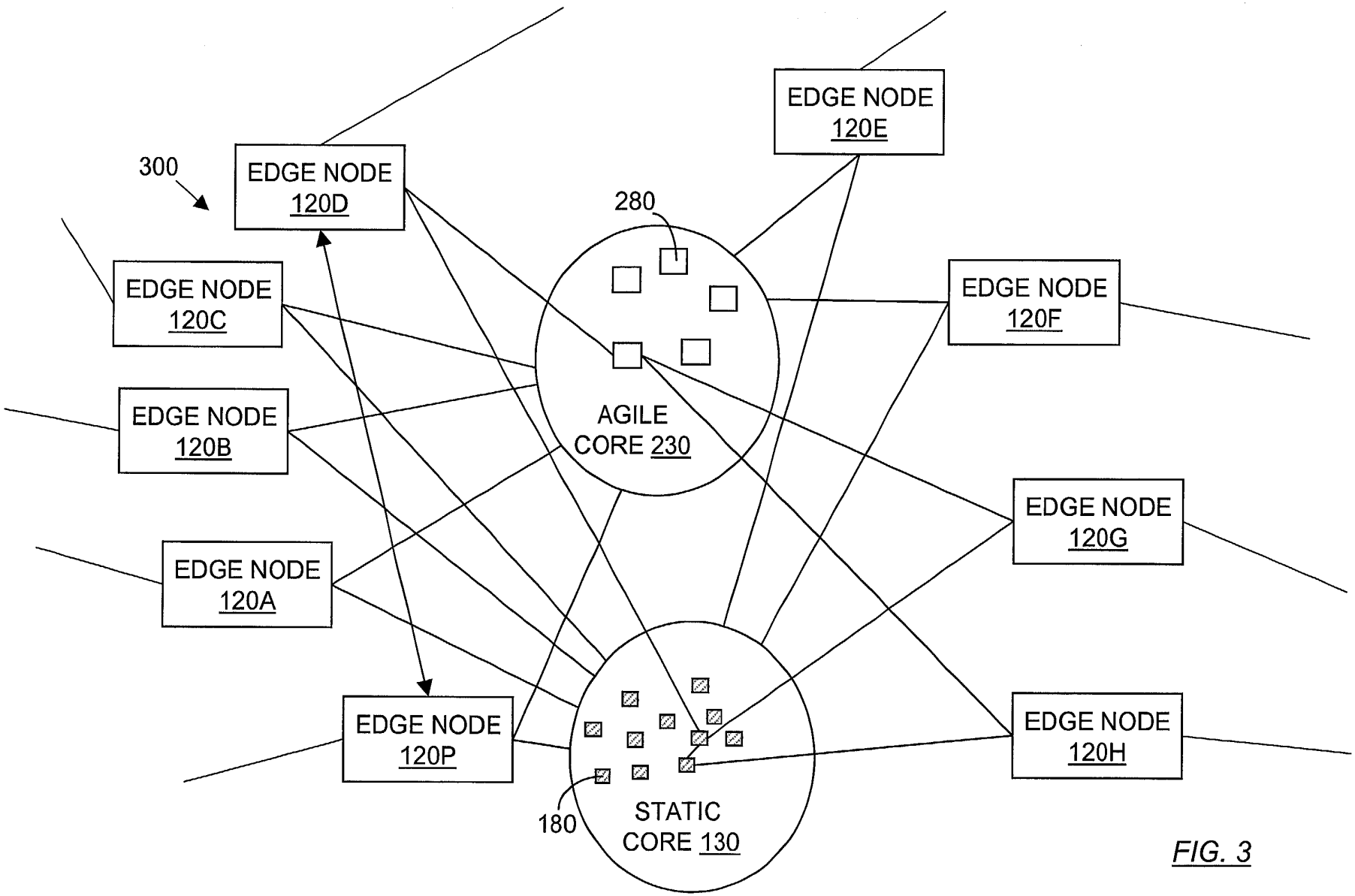
300
EDGE NODE 120D
EDGE NODE 120E
280
EDGE NODE 120C
EDGE NODE 120F
EDGE NODE 120B
AGILE CORE 230
EDGE NODE 120G
EDGE NODE 120A
EDGE NODE 120P
EDGE NODE 120H
180
STATIC CORE 130

FIG. 3

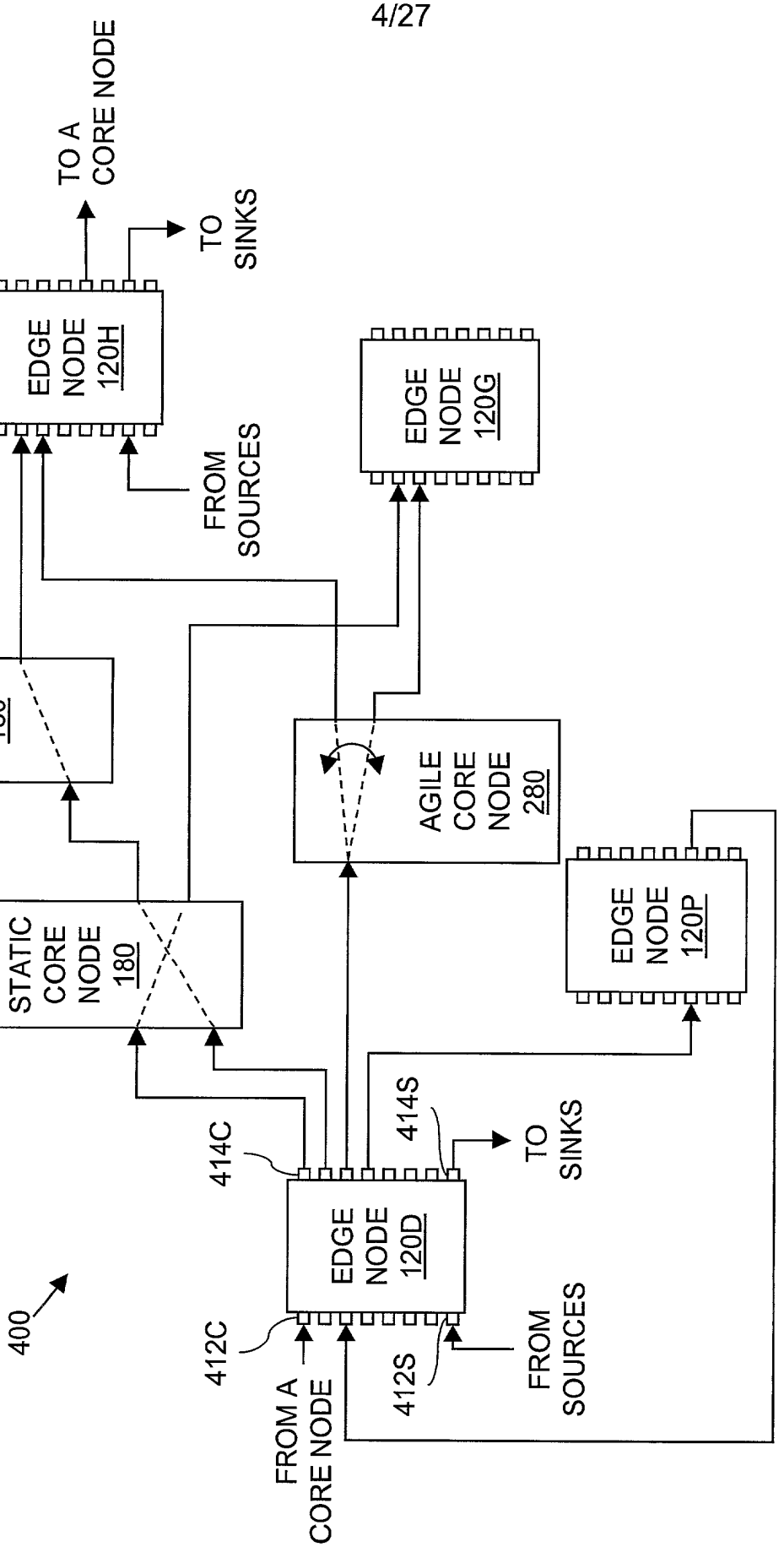
400
EDGE NODE 120D
412C
412S
414C
414S
FROM A CORE NODE
FROM SOURCES
TO SINKS
STATIC CORE NODE 180
STATIC CORE NODE 180
AGILE CORE NODE 280
EDGE NODE 120P
EDGE NODE 120G
EDGE NODE 120H
FROM SOURCES
TO SINKS
TO A CORE NODE

FIG. 4

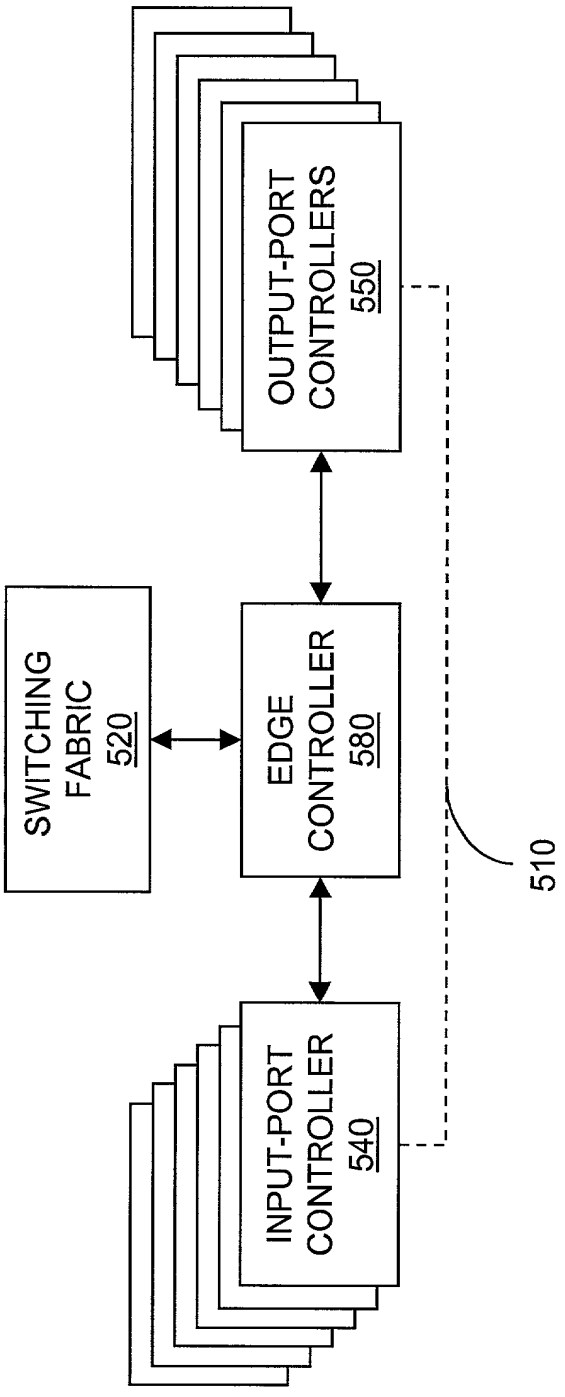
OUTPUT-PORT CONTROLLERS 550
SWITCHING FABRIC 520
EDGE CONTROLLER 580
INPUT-PORT CONTROLLER 540
510

FIG. 5

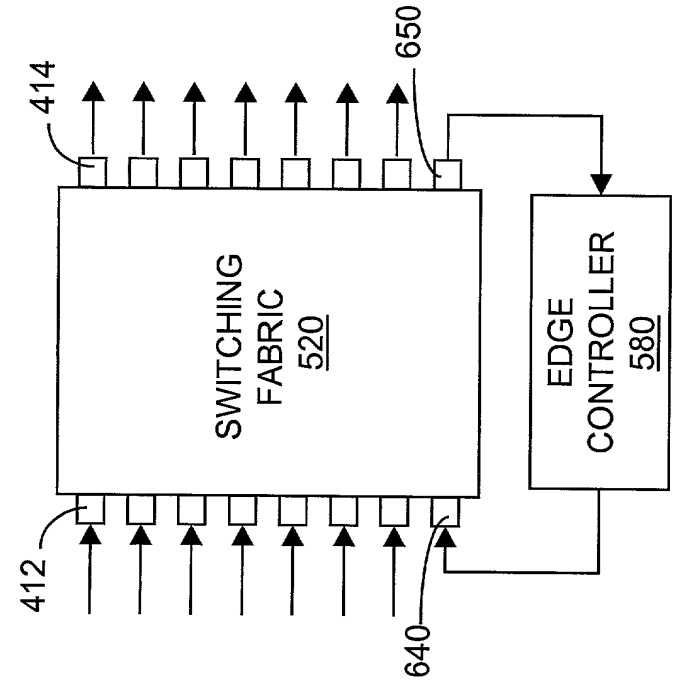
414
650
SWITCHING FABRIC 520
EDGE CONTROLLER 580
412
640

FIG. 6B

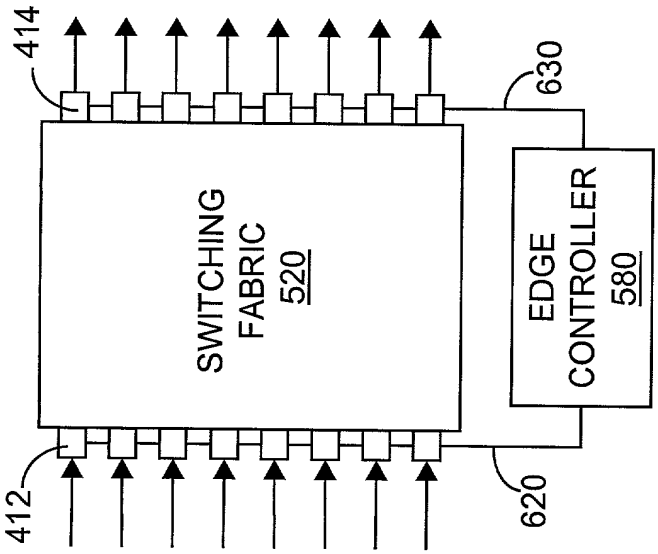
414
630
SWITCHING FABRIC 520
EDGE CONTROLLER 580
412
620

FIG. 6A

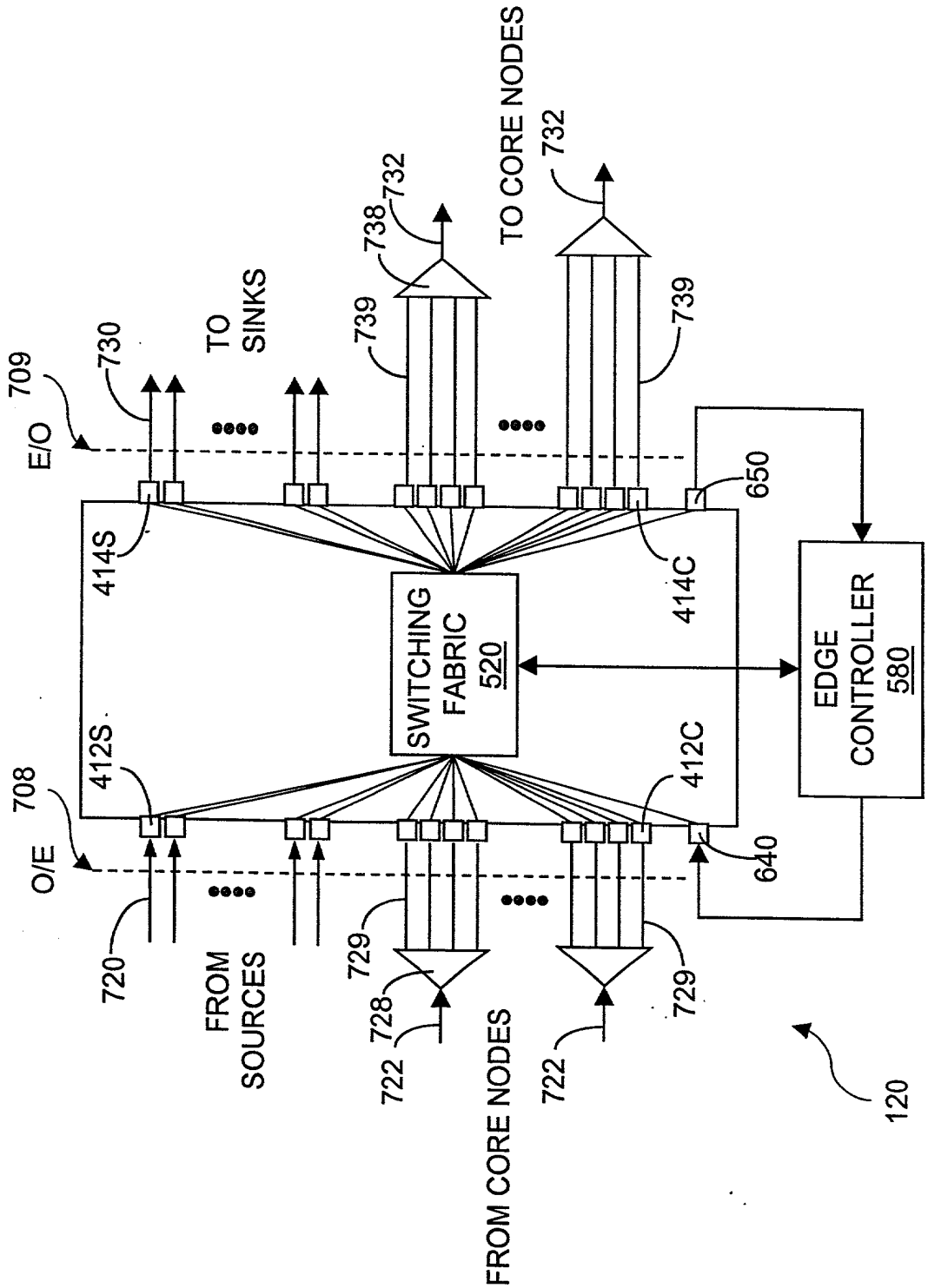
709
E/O
730
TO SINKS
739
738
732
TO CORE NODES
732
739
650
414S
414C
SWITCHING FABRIC 520
EDGE CONTROLLER 580
412S
412C
708
O/E
640
720
FROM SOURCES
729
728
722
FROM CORE NODES
722
729
120

FIG. 7

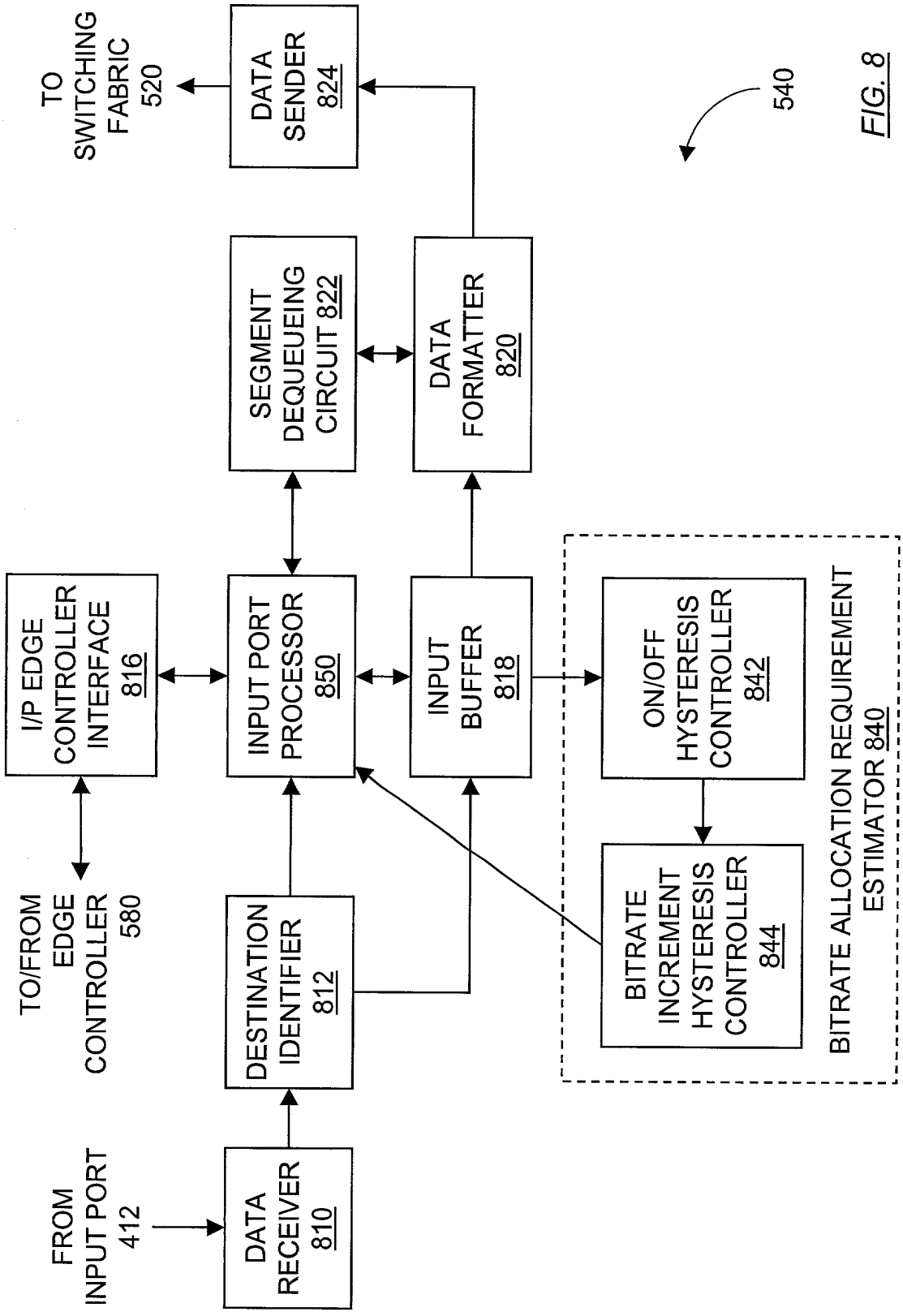
FROM INPUT PORT 412
DATA RECEIVER 810
DESTINATION IDENTIFIER 812
TO/FROM EDGE CONTROLLER 580
I/P EDGE CONTROLLER INTERFACE 816
INPUT PORT PROCESSOR 850
INPUT BUFFER 818
SEGMENT DEQUEUEING CIRCUIT 822
DATA FORMATTER 820
DATA SENDER 824
TO SWITCHING FABRIC 520
ON/OFF HYSTERESIS CONTROLLER 842
BITRATE INCREMENT HYSTERESIS CONTROLLER 844
BITRATE ALLOCATION REQUIREMENT ESTIMATOR 840
540

FIG. 8

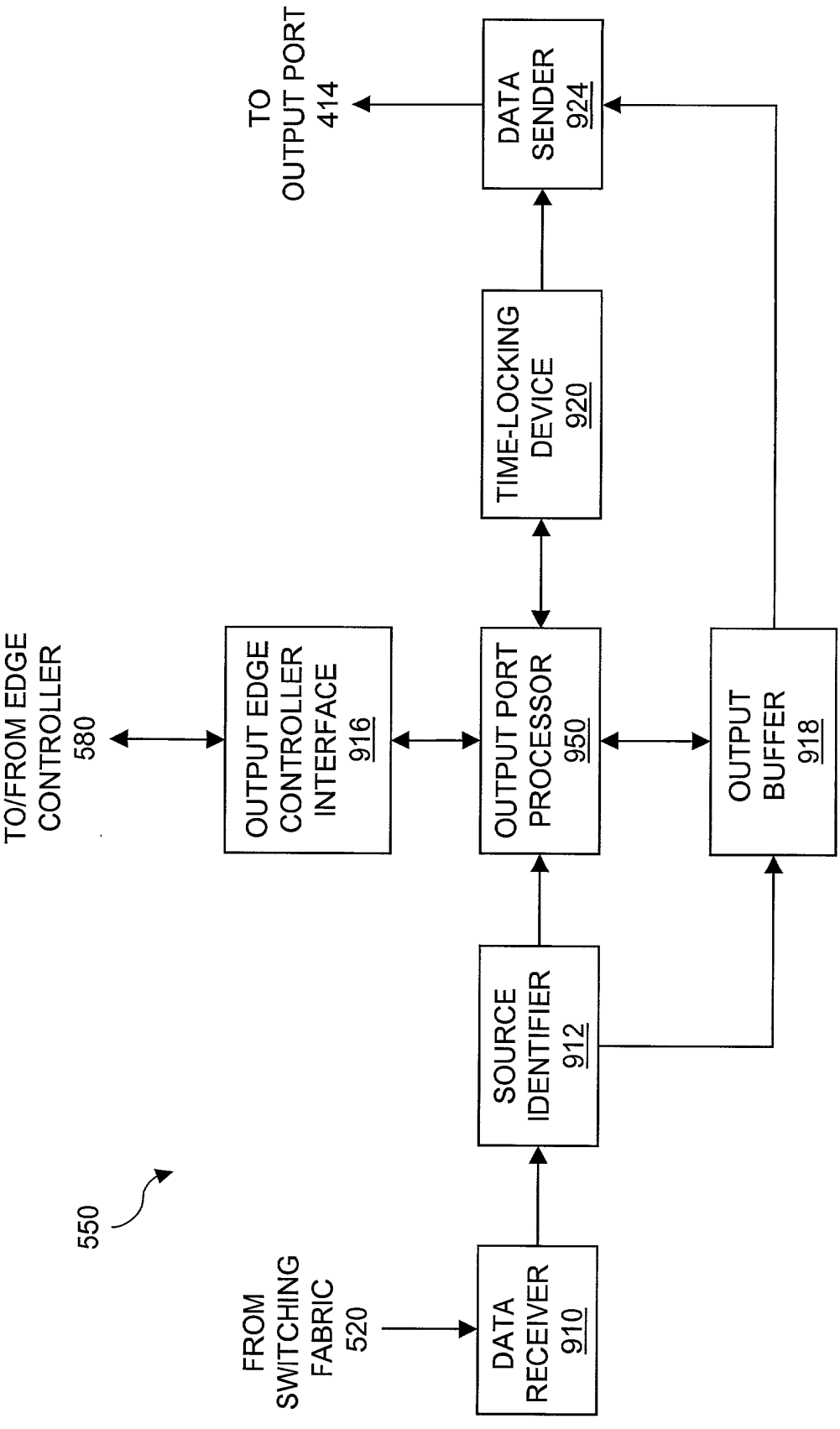
550
FROM SWITCHING FABRIC 520
DATA RECEIVER 910
SOURCE IDENTIFIER 912
OUTPUT PORT PROCESSOR 950
OUTPUT BUFFER 918
OUTPUT EDGE CONTROLLER INTERFACE 916
TO/FROM EDGE CONTROLLER 580
TIME-LOCKING DEVICE 920
DATA SENDER 924
TO OUTPUT PORT 414

FIG. 9

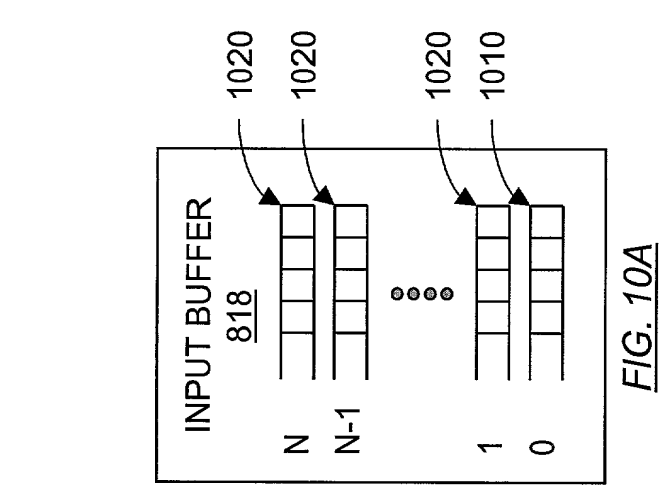

FIG. 10A

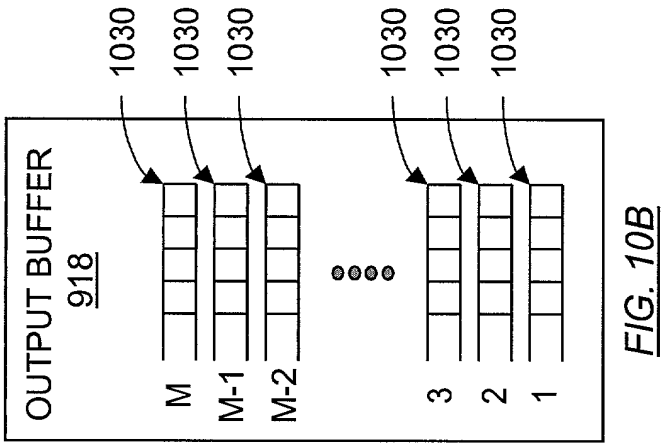

FIG. 10B

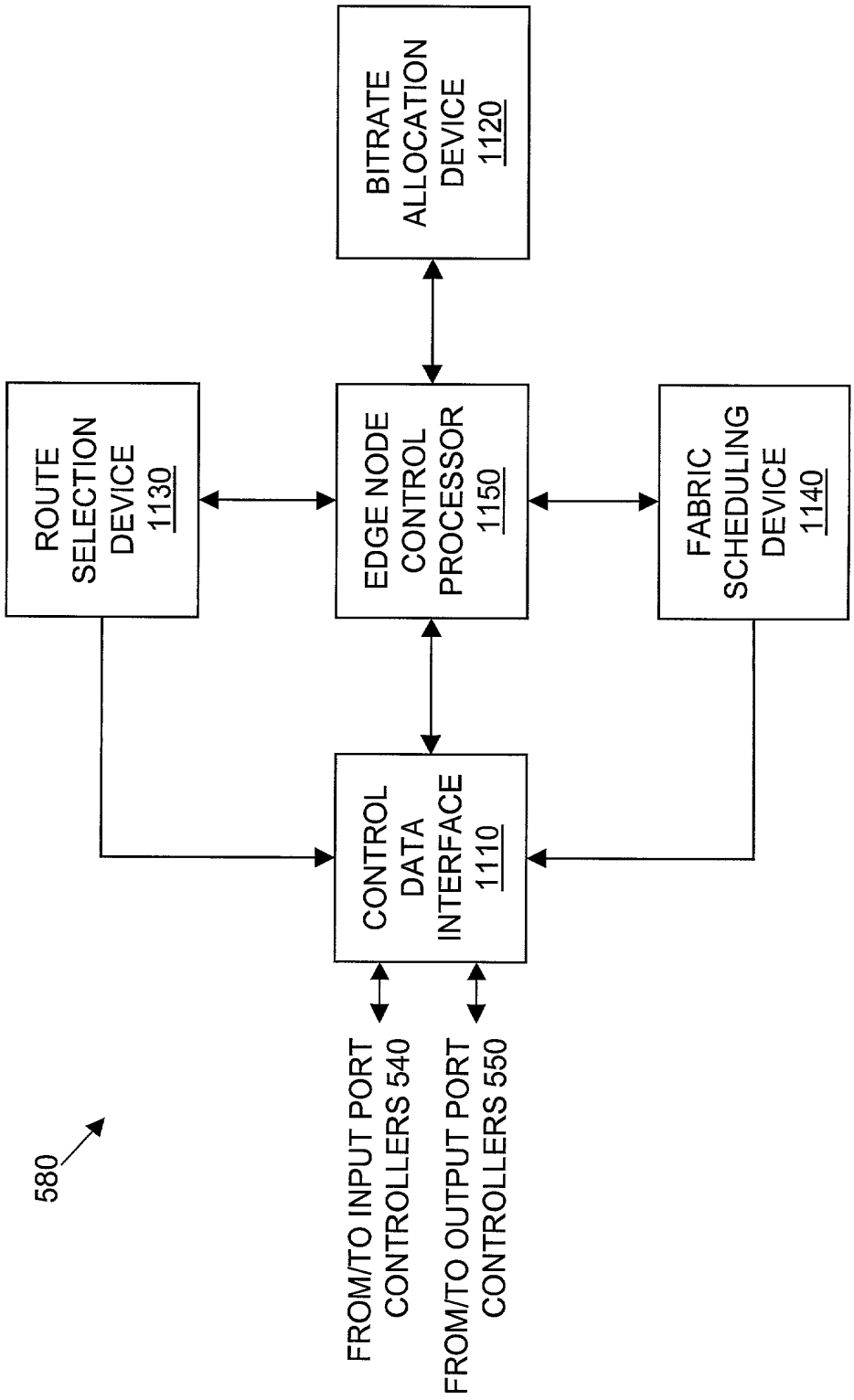
580
FROM/TO INPUT PORT CONTROLLERS 540
FROM/TO OUTPUT PORT CONTROLLERS 550
CONTROL DATA INTERFACE 1110
ROUTE SELECTION DEVICE 1130
EDGE NODE CONTROL PROCESSOR 1150
FABRIC SCHEDULING DEVICE 1140
BITRATE ALLOCATION DEVICE 1120

FIG. 11

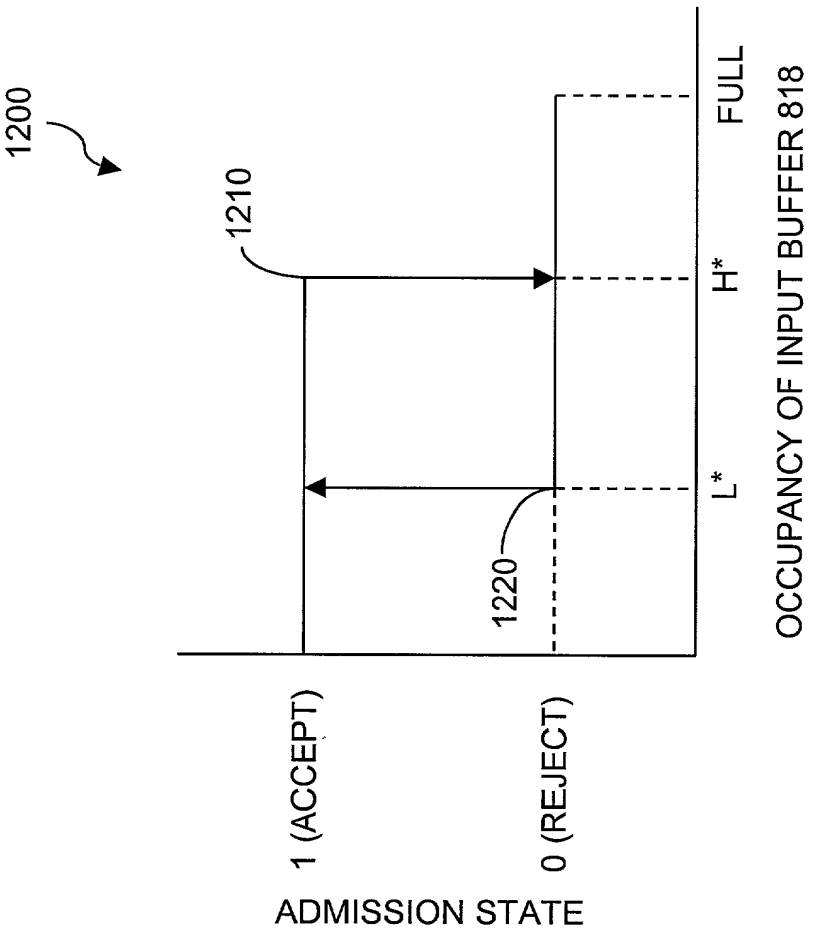
1200
1210
1220
L*
H*
FULL
OCCUPANCY OF INPUT BUFFER 818
1 (ACCEPT)
0 (REJECT)
ADMISSION STATE

FIG. 12

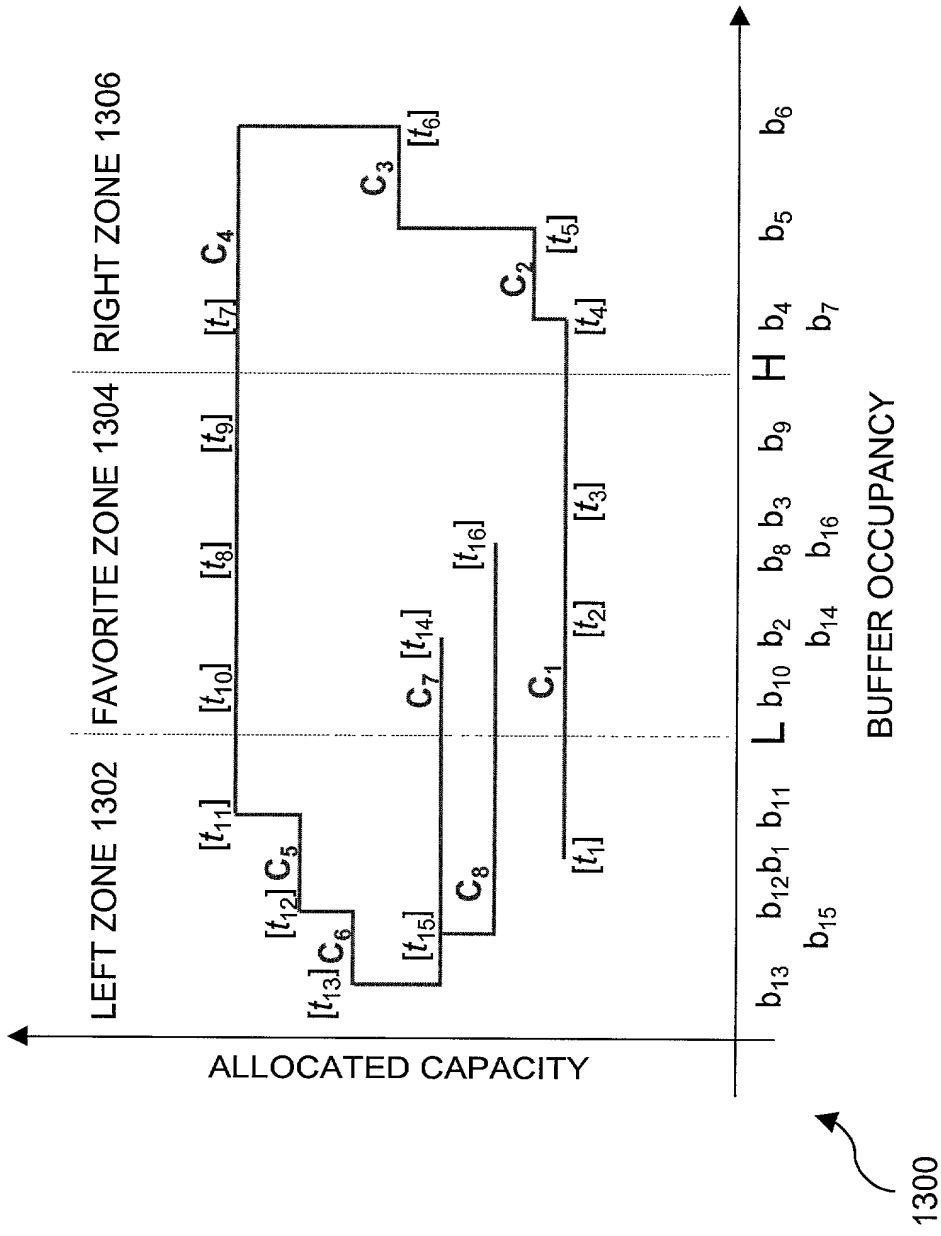
LEFT ZONE 1302
FAVORITE ZONE 1304
RIGHT ZONE 1306
ALLOCATED CAPACITY
BUFFER OCCUPANCY
L
H
b_{13} b_{12} b_1 b_{11} b_{10} b_2 b_8 b_3 b_9 b_4 b_6
b_{15} b_{14} b_{16} b_7
b_5
$[t_{11}]$ $[t_{10}]$ $[t_8]$ $[t_9]$ $[t_7]$ C_4
C_3 $[t_6]$
C_2 $[t_5]$
$[t_4]$
$[t_{12}]$ C_5
$[t_{13}]$ C_6
C_7 $[t_{14}]$
$[t_{15}]$
C_8
$[t_{16}]$
C_1
$[t_2]$ $[t_3]$
$[t_1]$
1300

FIG. 13

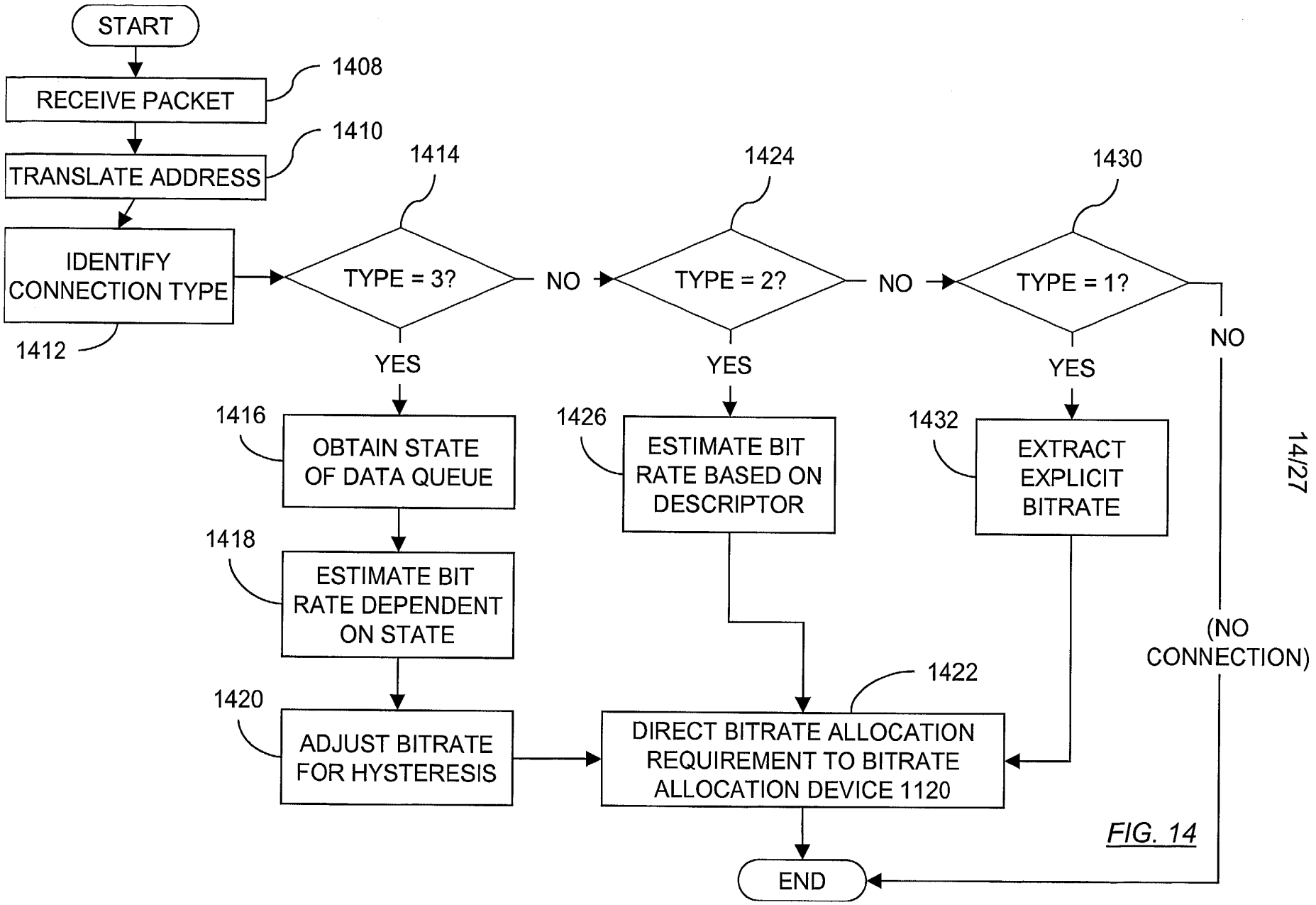
START
RECEIVE PACKET
1408
TRANSLATE ADDRESS
1410
IDENTIFY CONNECTION TYPE
1412
1414
TYPE = 3?
NO
1424
TYPE = 2?
NO
1430
TYPE = 1?
NO
YES
YES
YES
1416
OBTAIN STATE OF DATA QUEUE
1418
ESTIMATE BIT RATE DEPENDENT ON STATE
1420
ADJUST BITRATE FOR HYSTERESIS
1426
ESTIMATE BIT RATE BASED ON DESCRIPTOR
1432
EXTRACT EXPLICIT BITRATE
1422
DIRECT BITRATE ALLOCATION REQUIREMENT TO BITRATE ALLOCATION DEVICE 1120
(NO CONNECTION)
END

FIG. 14

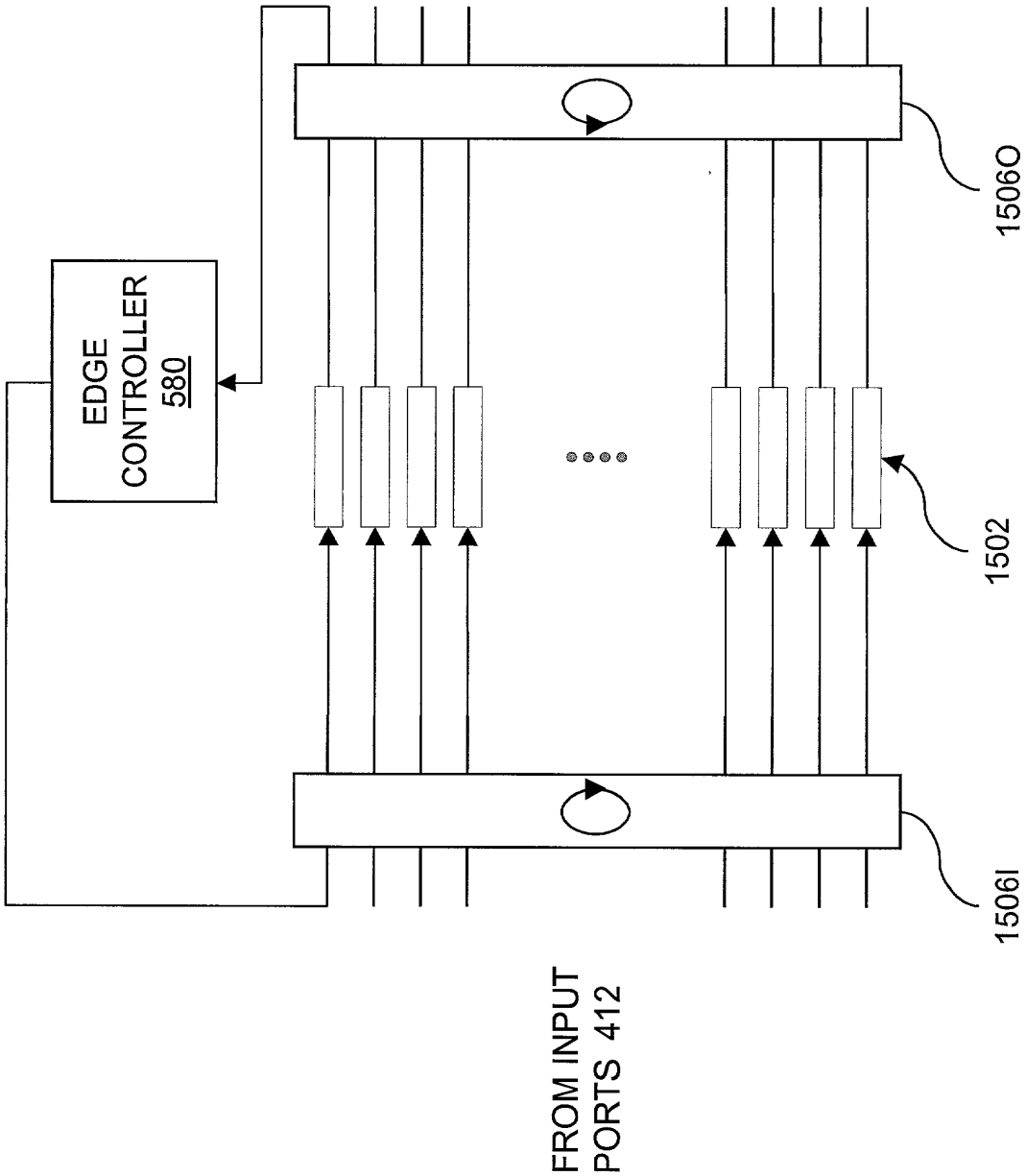
EDGE CONTROLLER 580
TO OUTPUT PORTS 414
FROM INPUT PORTS 412
1506O
1502
1506I

FIG. 15A

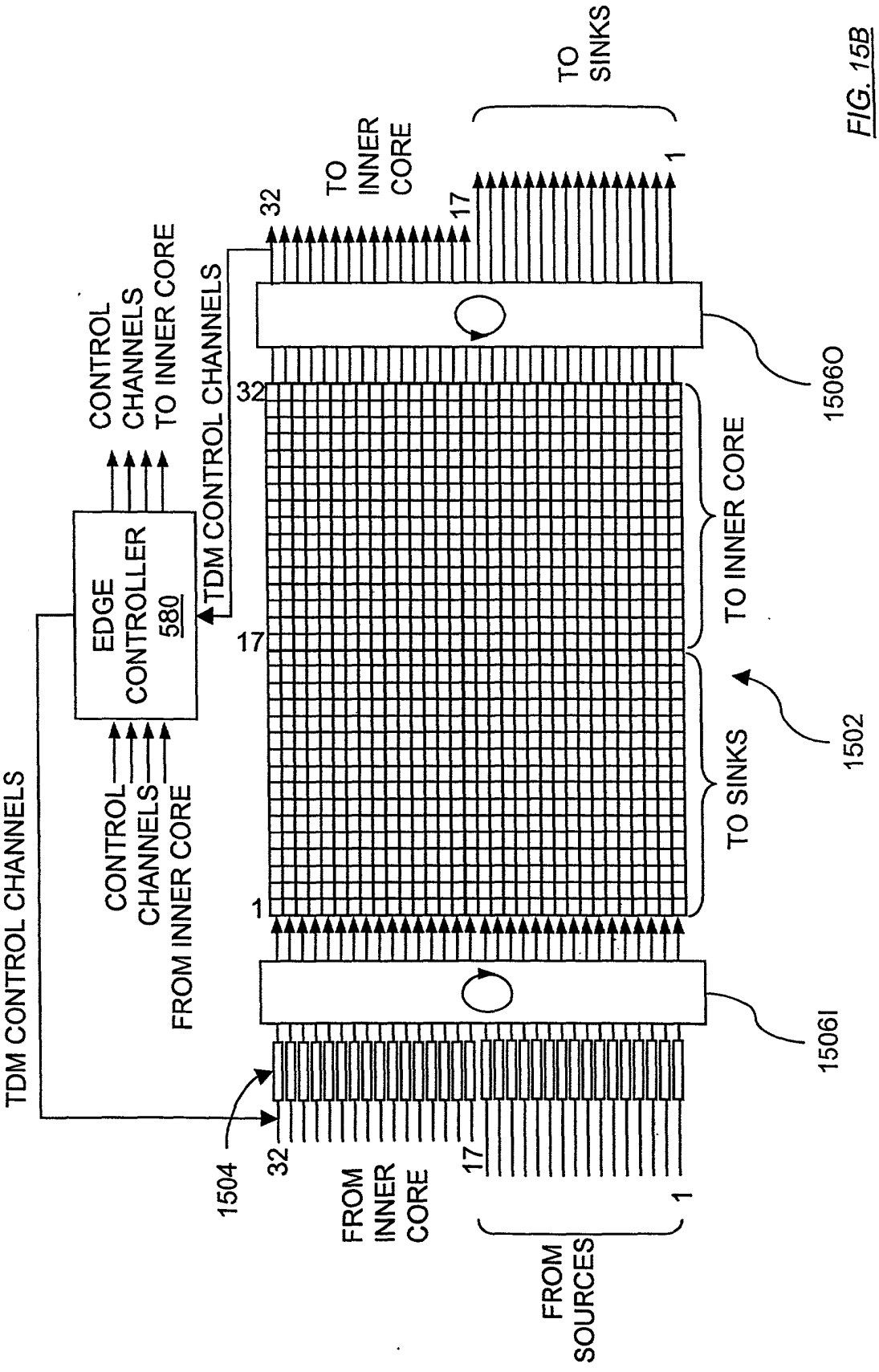
TDM CONTROL CHANNELS
EDGE CONTROLLER 580
CONTROL CHANNELS FROM INNER CORE
CONTROL CHANNELS TO INNER CORE
TDM CONTROL CHANNELS
1504
32
17
1
FROM INNER CORE
FROM SOURCES
1506I
1502
TO INNER CORE
TO SINKS
1506O
TO INNER CORE
TO SINKS

FIG. 15B

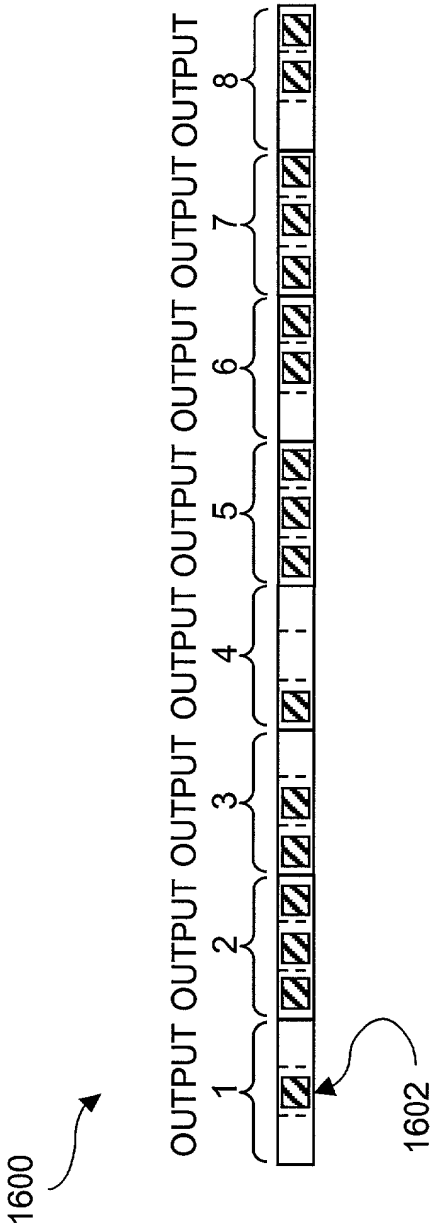
1600
OUTPUT OUTPUT OUTPUT OUTPUT OUTPUT OUTPUT OUTPUT OUTPUT
1
2
3
4
5
6
7
8
1602

FIG. 16

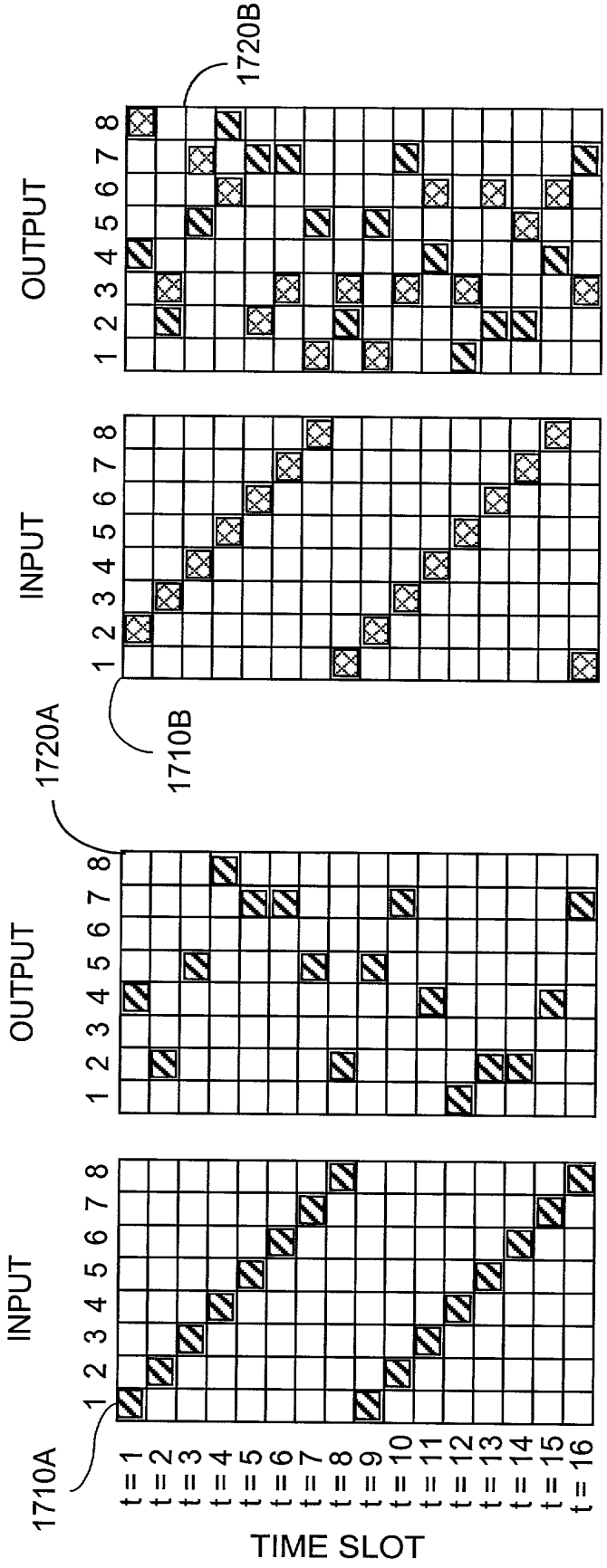

FIG. 17A

FIG. 17B

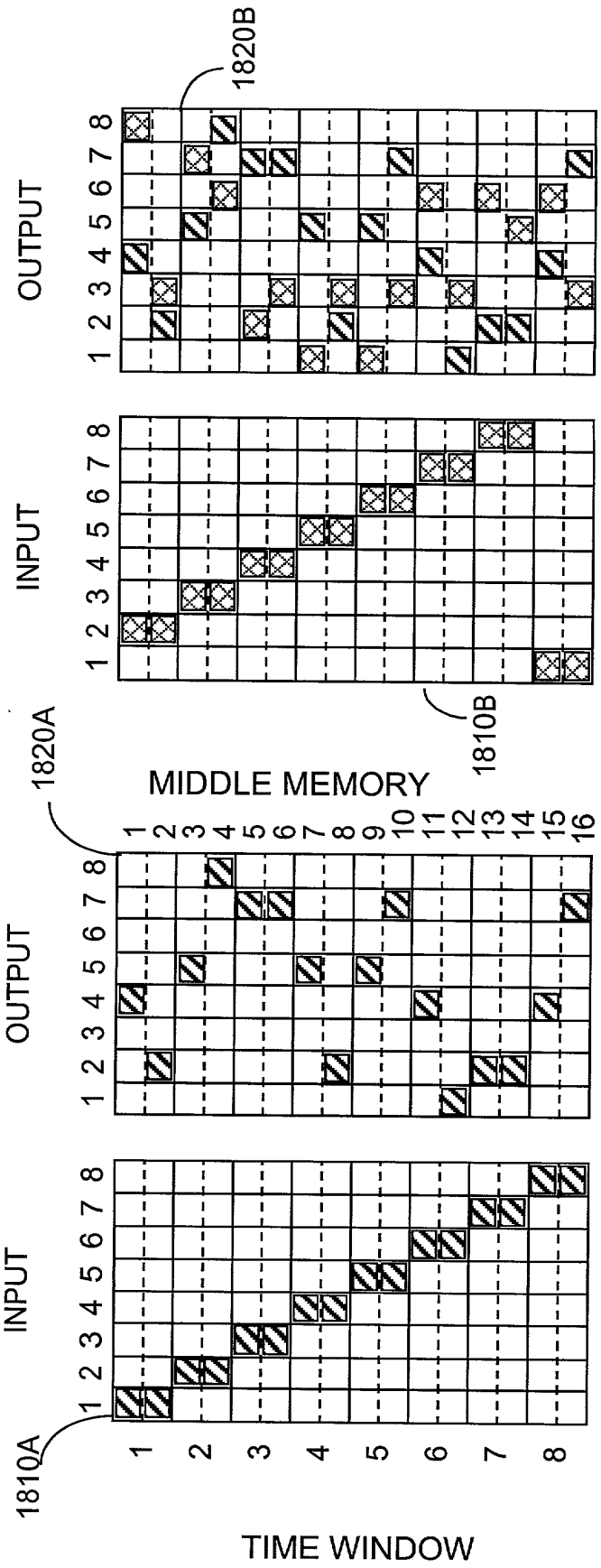

FIG. 18B

FIG. 18A

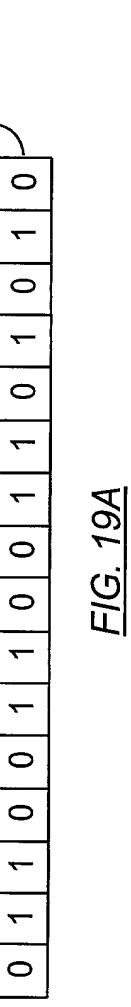

FIG. 19A

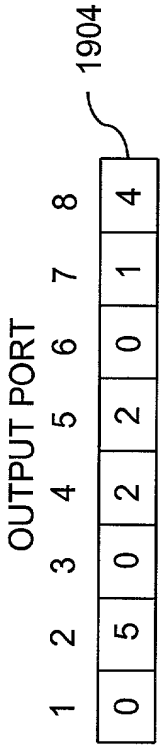

FIG. 19B

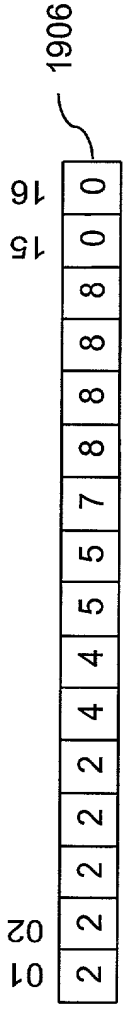

FIG. 19C

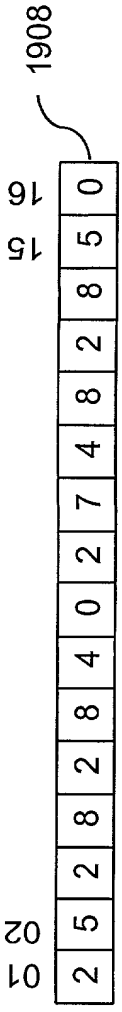

FIG. 19D

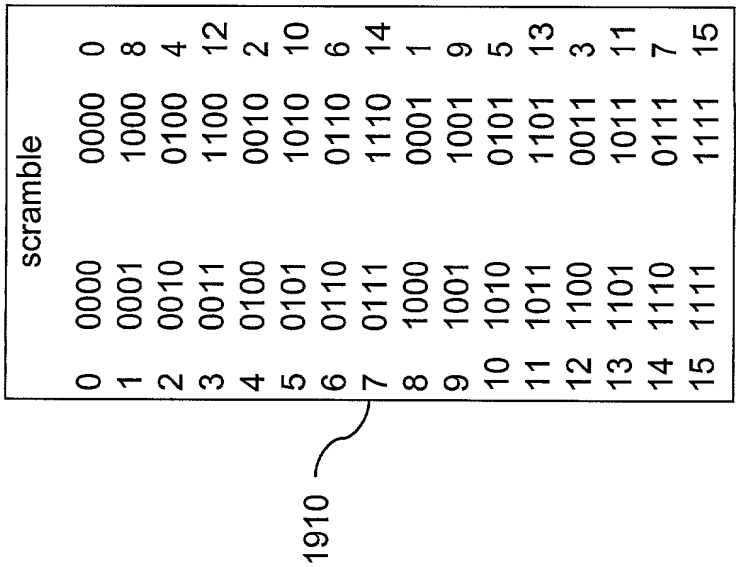

FIG. 19E

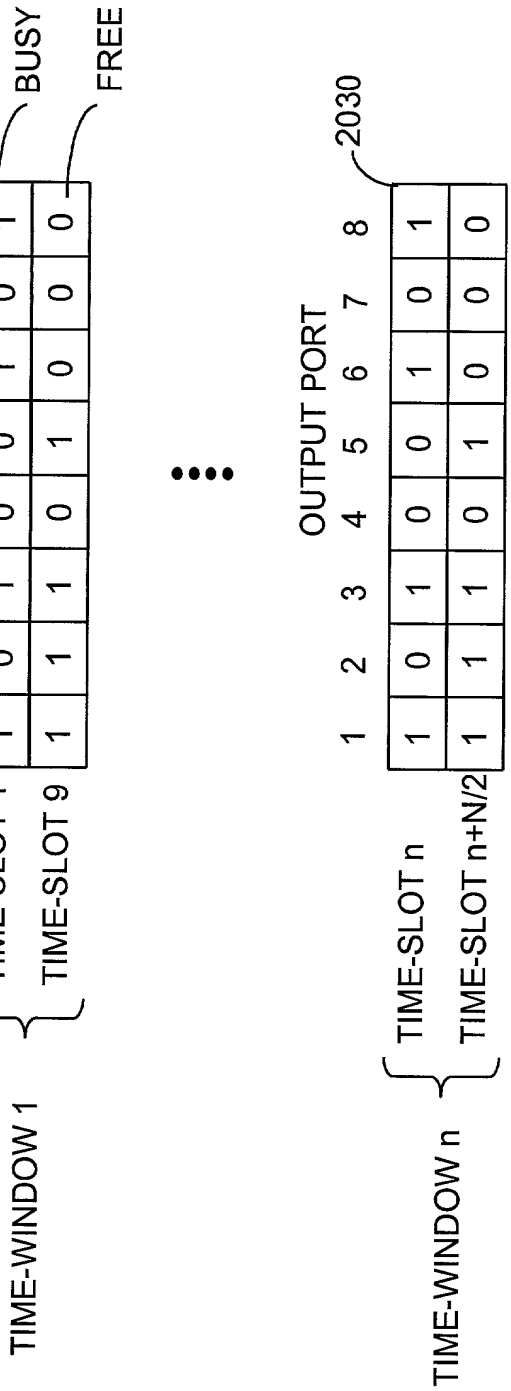
OUTPUT PORT
1 2 3 4 5 6 7 8
2030
BUSY
FREE
TIME-WINDOW 1
TIME-SLOT 1
TIME-SLOT 9
1 0 1 0 0 1 0 1
1 1 1 0 1 0 0 0
TIME-WINDOW n
TIME-SLOT n
TIME-SLOT n+N/2
1 0 1 0 0 1 0 1
1 1 1 0 1 0 0 0

FIG. 20

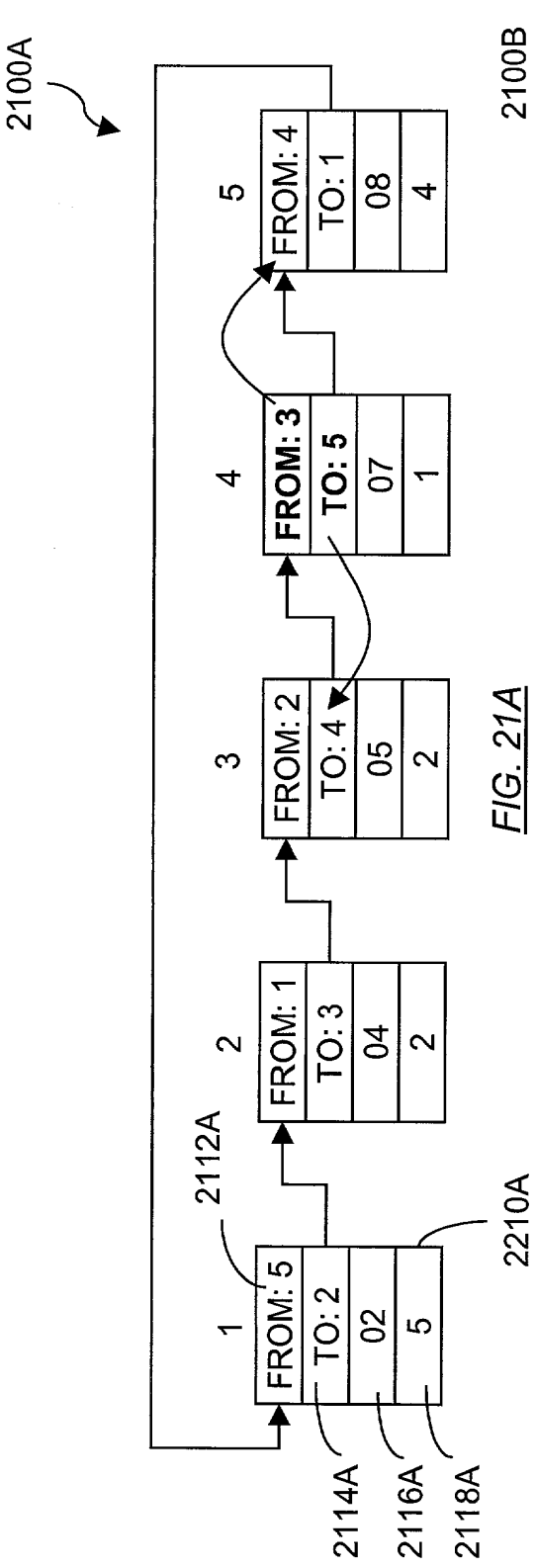

FIG. 21A

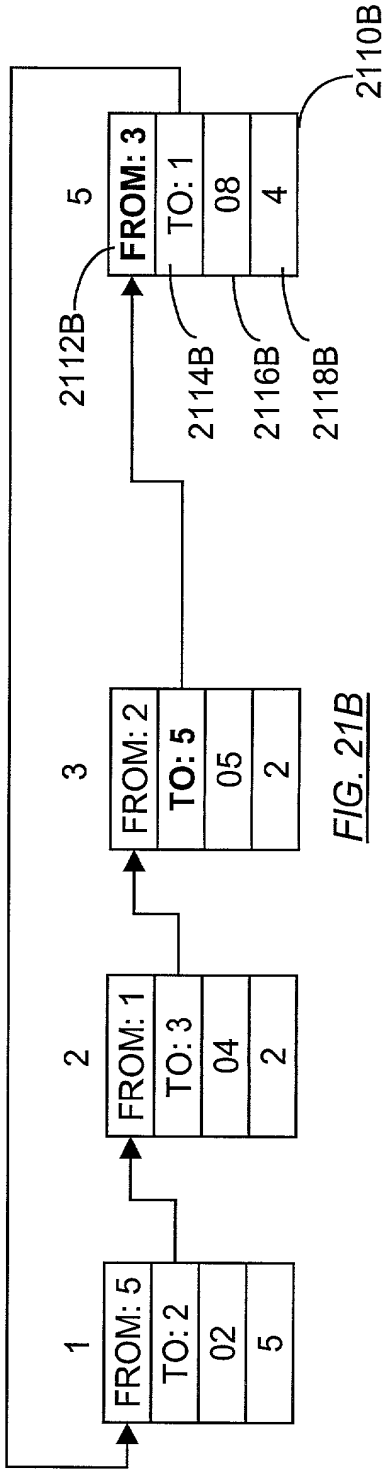

FIG. 21B

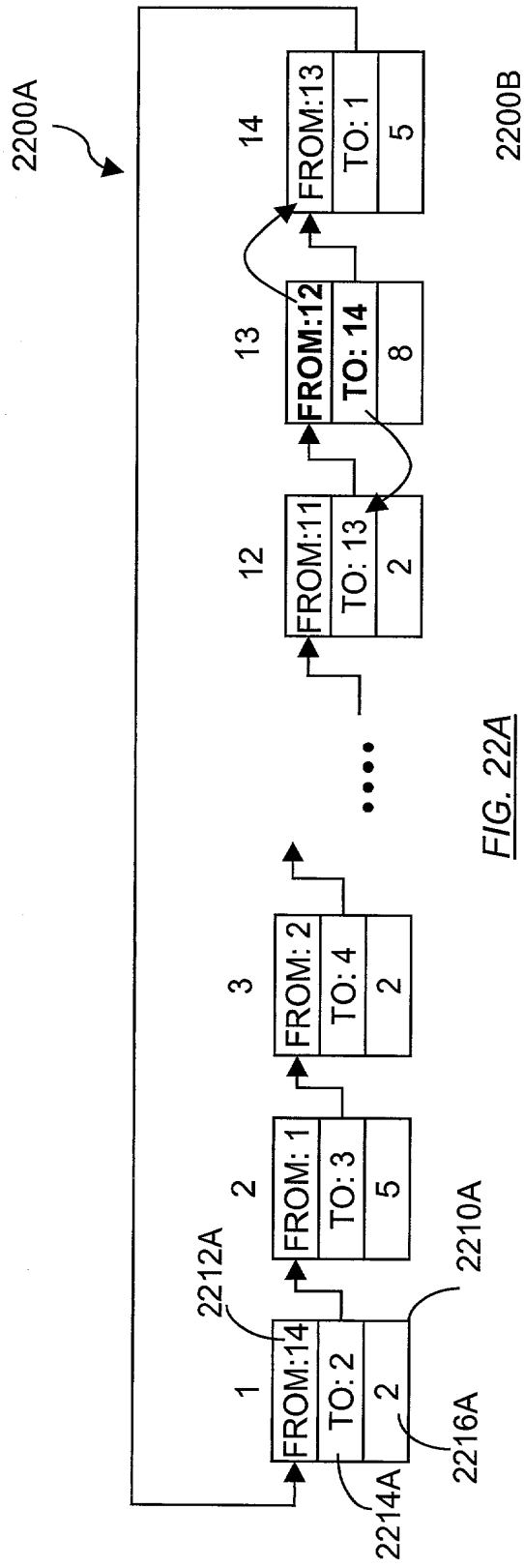

FIG. 22A

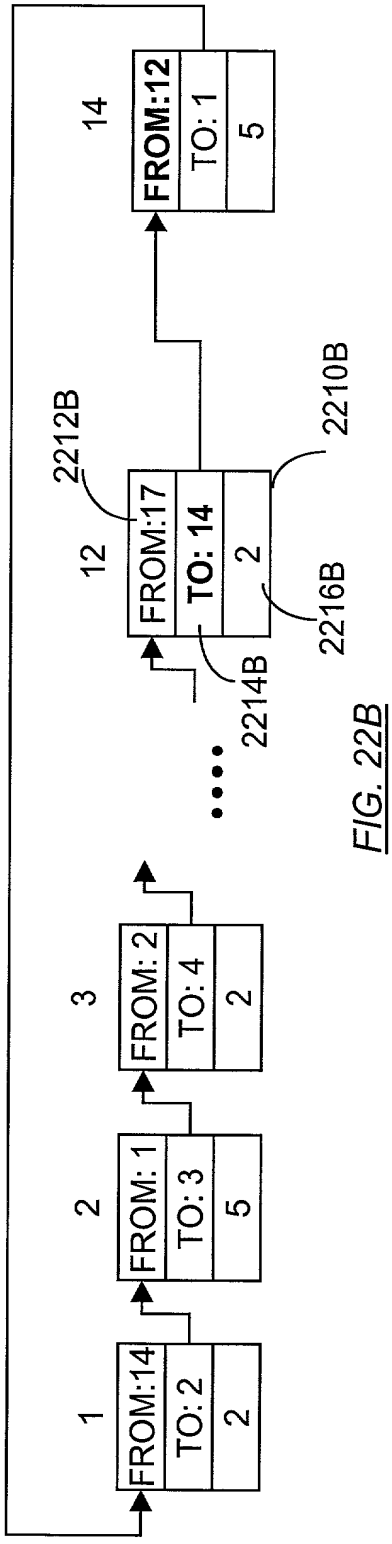

FIG. 22B

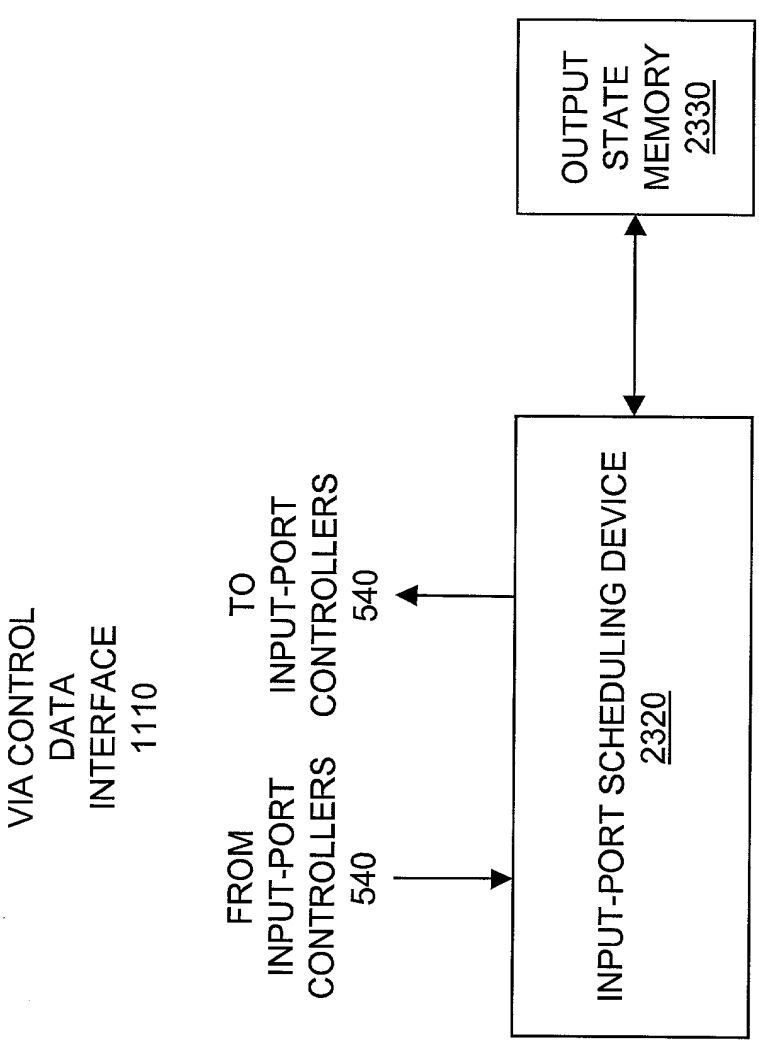
VIA CONTROL DATA INTERFACE 1110
FROM INPUT-PORT CONTROLLERS 540
TO INPUT-PORT CONTROLLERS 540
INPUT-PORT SCHEDULING DEVICE 2320
OUTPUT STATE MEMORY 2330

FIG. 23

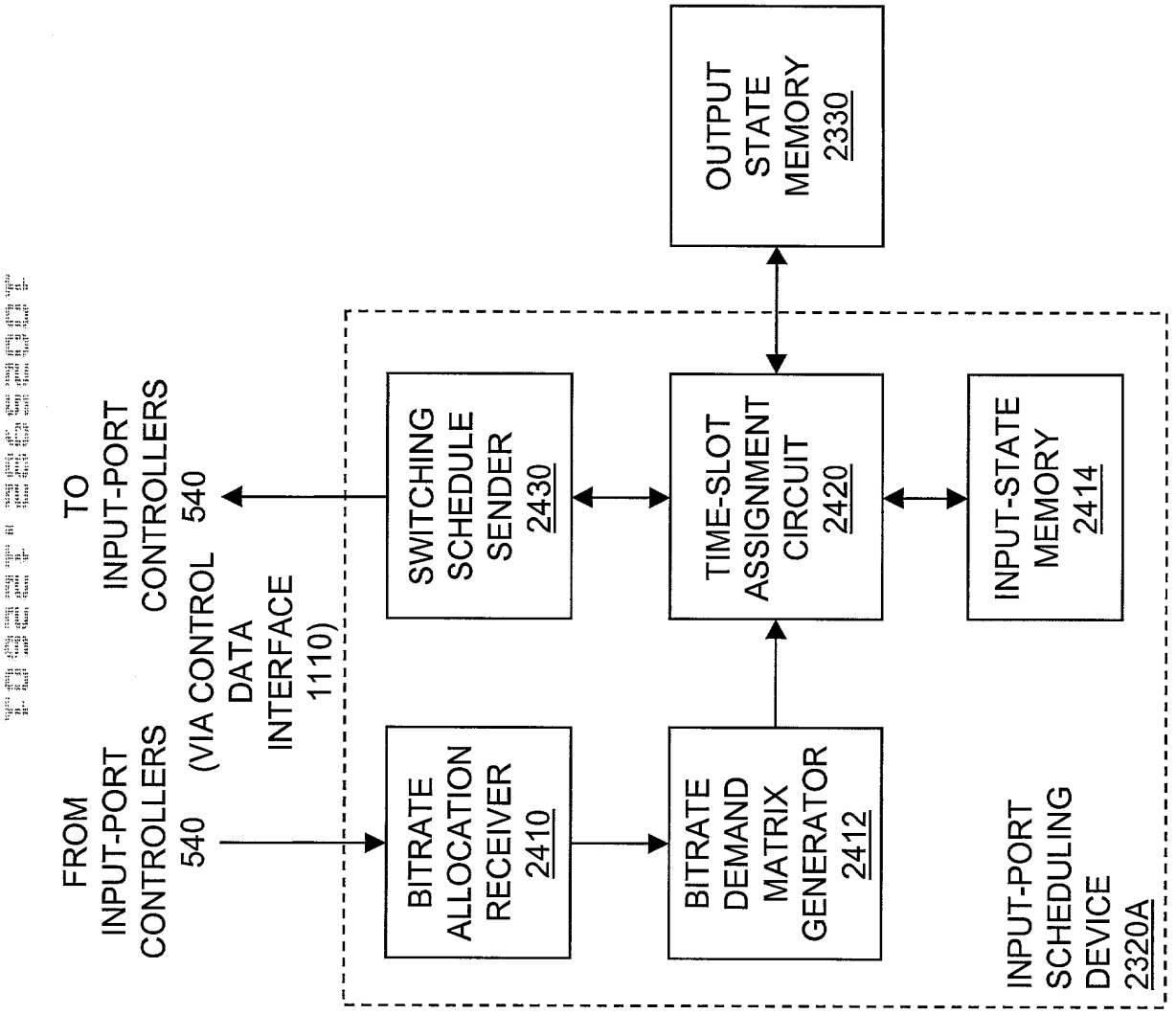
FROM INPUT-PORT CONTROLLERS 540
(VIA CONTROL DATA INTERFACE 1110)
TO INPUT-PORT CONTROLLERS 540
BITRATE ALLOCATION RECEIVER 2410
BITRATE DEMAND MATRIX GENERATOR 2412
SWITCHING SCHEDULE SENDER 2430
TIME-SLOT ASSIGNMENT CIRCUIT 2420
INPUT-STATE MEMORY 2414
OUTPUT STATE MEMORY 2330
INPUT-PORT SCHEDULING DEVICE 2320A

FIG. 24

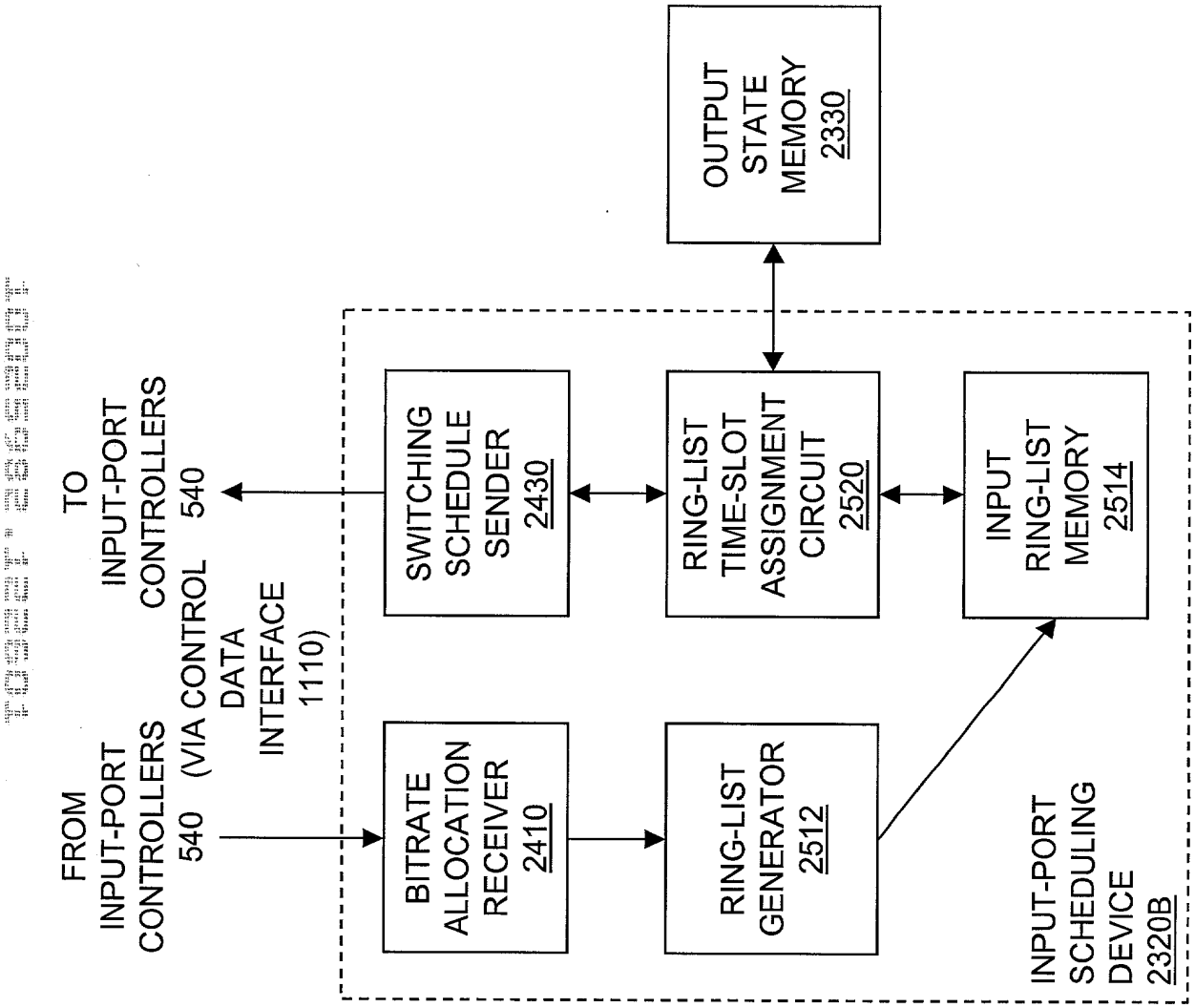
FROM INPUT-PORT CONTROLLERS 540
TO INPUT-PORT CONTROLLERS 540 (VIA CONTROL DATA INTERFACE 1110)
BITRATE ALLOCATION RECEIVER 2410
SWITCHING SCHEDULE SENDER 2430
RING-LIST GENERATOR 2512
RING-LIST TIME-SLOT ASSIGNMENT CIRCUIT 2520
INPUT RING-LIST MEMORY 2514
OUTPUT STATE MEMORY 2330
INPUT-PORT SCHEDULING DEVICE 2320B

FIG. 25

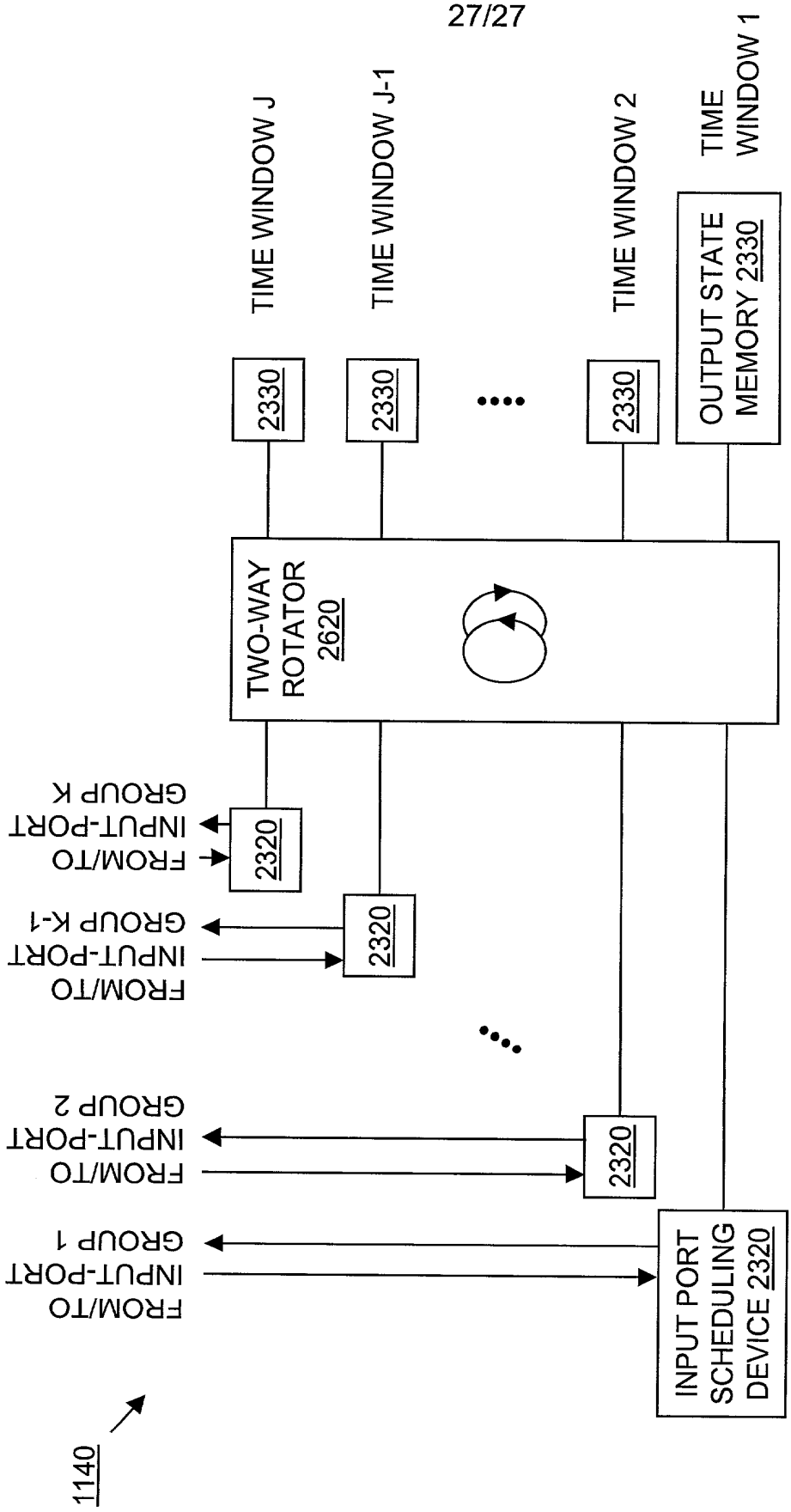
1140
FROM/TO INPUT-PORT GROUP 1
FROM/TO INPUT-PORT GROUP 2
FROM/TO INPUT-PORT GROUP K-1
FROM/TO INPUT-PORT GROUP K
INPUT PORT SCHEDULING DEVICE 2320
2320
2320
2320
2320
TWO-WAY ROTATOR 2620
2330
2330
2330
OUTPUT STATE MEMORY 2330
TIME WINDOW J
TIME WINDOW J-1
TIME WINDOW 2
TIME WINDOW 1

FIG. 26